
STUDY OF LOW-SIGNAL AMPLIFIERS WITH FIELD-EFFECT TRANSISTORS

■ **Abstract:**

In this work are presented the types of amplifier stages with field-effect transistors, as well as the diagrams of the low-signal amplifiers achieved with TEC-J for the three connection types: common-source, common-grid and common-drain. Also, using the EWB-Multisim 8 program, it was simulated the operation of the amplifier with TEC-J in common-source connection, the amplifier with TEC-MOS in common-drain connection and the cascode amplifier with two TEC-J transistors .

■ **Keywords:**

TEC transistor, Voltage amplification, Current amplification, Amplifier, Simulation, Multisim 8

■ **INTRODUCTION**

The models which describe the operation at small signal variations have in view a description of the transistors' behavior in applications of amplifier stages' type. In these applications, the transistors are polarized in the characteristics' area where these are almost horizontal lines; against the collector, the transistors are equivalent with a controlled current generator and behave linearly. In the respective circuits' operation, the effect of the charges accumulated in junctions or other regions of the transistors is the one of some capacitors which produce phase differences and dampings with frequency.

The small signal variations are the voltage and current variations situated within an interval relatively restricted around some continuous components, interval where the device's behavior can be described by linear equations.

The device's equivalent diagram is composed by linear components, of which values depend generally to the operation static point (the continuous components of voltages and currents through the device). The voltage and current variations are small, but the time-variation speeds are not neglectable, thereby the accumulations of electric charges in the device should be taken in consideration

■ **TEC-J and TEC-MOS BEHAVIOR AT SMALL SIGNAL VARIATIONS**

The operation static point should be in the saturation region of the drain current (Fig. 1). In this operation regime, the equation of the TEC-J transistor is:

$$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1)$$

$$dI_D = 2 I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_P}\right) \cdot \left(-\frac{dV_{GS}}{V_P}\right) = 2 I_{DSS} \cdot \sqrt{\frac{I_D}{I_{DSS}}} \cdot \left(-\frac{dV_{GS}}{V_P}\right) \quad (2)$$

Using the same convention to note the variations and the components $v_{GS} = V_{GS} + v_{gs}$ and $i_D = I_D + i_d$, we have the correspondence:

$$dI_D \rightarrow i_d \text{ and } dV_{GS} \rightarrow v_{gs} \quad (3)$$

$$i_d = -2 \frac{\sqrt{I_D I_{DSS}}}{V_P} \cdot v_{gs} \quad (4)$$

The TEC-J transistor's slope is:

$$g_m = \frac{i_d}{v_{gs}} \Big|_{V_{DS}=\text{constant}} = -2 \frac{\sqrt{I_D I_{DSS}}}{V_P} \quad (5)$$

The higher the drain current, the higher the slope. The maximum slope of a TEC-J is obtained at $V_{GS} = 0$ and has the value:

$$(g_m)_{\max} = |2 I_{DSS} / V_P| \quad (6)$$

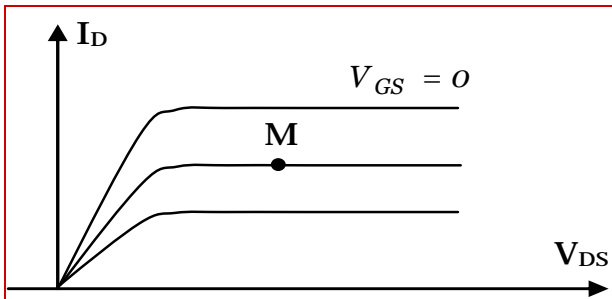


Fig. 1. TEC-J's operation point as amplifier

The small variations $v_{gs} > 0$ of the grid-source voltage produce the following effects:

- ✚ the drain current's increase due to the increase of the channel's conductance (the channels' area increases);
- ✚ the electric charge accumulated in the passing region of the grid-channel junction modifies in the source's region and, as result, is necessary a grid current to supply this modification $i'_g = C_{gs} \cdot \frac{dv_{gs}}{dt}$ where C_{gs} is the barrier capacity of the grid-channel junction in the source's area;

- ✚ the drain-source voltage modifies (following the modification of the drain current), which leads to the modification of the electric charge accumulated in the passing region of the grid-channel junction in the drain's region; a grid current is necessary to supply this charge modification $i''_g = C_{gd} \cdot \frac{dv_{gd}}{dt}$ where C_{gd} is the barrier capacity of the grid-channel junction in the drain's area.

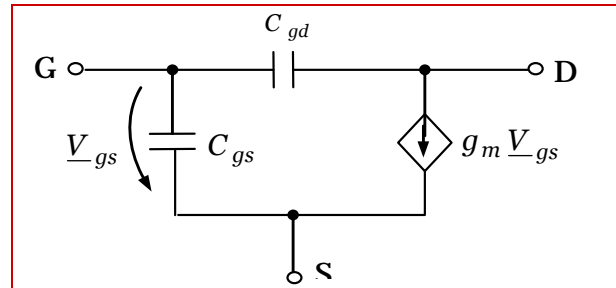


Fig. 2. TEC-J's equivalent diagram

TEC-MOS behavior is described by an equivalent diagram identical with the one from Fig. 2. Capacities C_{gs} and C_{gd} correspond to the TEC-MOS' sublayer grid capacities in the source's, respectively the drain's area. The TEC-MOS' equivalent slope is obtained starting from the transistor's equation in the drain current's saturation area.

$$I_D = k \cdot (V_{GS} - V_P)^2 \quad (7)$$

Is obtained the TEC-MOS transistor's slope:

$$g_m = 2 \sqrt{k I_D} \quad (8)$$

AMPLIFIER STAGES

The amplifier stage is the simplest constructive block of an amplifier. It contains one or maximum two transistors which operate in controlled current source regime. For TEC, this corresponds to the drain current's saturation area. Against the drain, the transistor behaves as a current generator controlled by the voltage V_{gs} . The three amplifier stages' types are based on the connections of the field-effect transistors:

- ✚ Common-source connection (Fig. 3);
- ✚ Common-grid connection (Fig. 4);
- ✚ Common-drain connection (Fig. 5).

The presented circuits include the resistances that ensure the transistors' polarization in the reminded regions. For the amplifier stages with

TEC are presented, for exemplification, only the diagrams of the stages with TEC-J, but there are similar circuits also for TEC-MOS.

In order to simplify the diagrams, in some cases it was chosen the option of polarization from two sources. In this case, the components' number from the diagram is smaller and the equivalent diagrams for small signal variations are simpler.

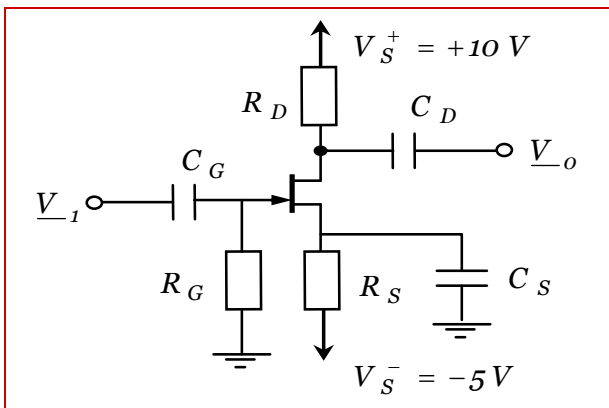


Fig. 3. Amplifier stage: Common-source

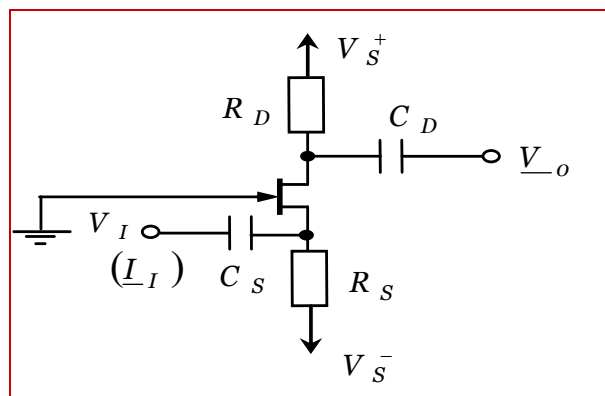


Fig. 4. Amplifier stage: Common-grid

Resistances R_G , R_S și R_D from the common-source amplifier stage (Fig. 3) ensures the TEC-J polarization in RAN. Capacitors C_G and C_D separate the input and output in d.c. from the TEC-J polarization and allow the coupling of the input and output signals, reason for which they are also called as coupling capacitors. The capacitor C_S , also called as decoupling capacitor, is short-circuiting to earth in a.c. the source TEC-J, where from the diagram's name. The resistance R_D has an important function also in a.c., as will be seen at amplification's calculation.

In the common-grid amplifier stage (Fig. 4), the TEC-J polarization in RAN is ensured by R_S and R_D and by the supply sources V_S^+ și V_S^- . The

coupling capacitors C_S and C_D are separating in d.c. the amplifier stage from the rest of the circuit, and allow the input's and output's coupling to the circuit.

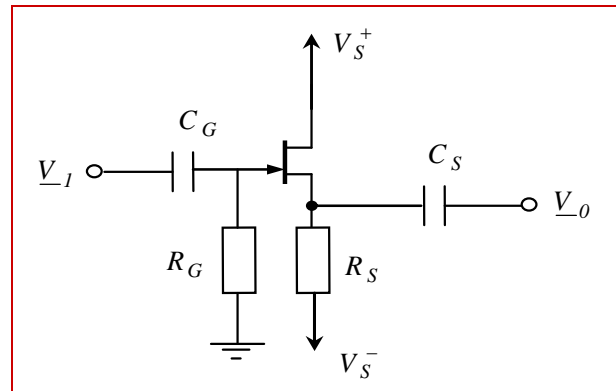


Fig. 5. Amplifier stage: Common-drain

The common-grid amplifier stage: (Fig. 5), also called as repeater-on-source, is polarized from the supply sources through the resistances R_G and R_S . The input and output coupling is achieved with the coupling capacitors C_G and C_S .

In all diagrams, the coupling and decoupling capacitors (C_G , C_D , C_S) should have sufficiently high values, in order that their impedances at operating frequencies to be considered neglectable, respectively the voltage drops on the equivalent impedances don't matter. This condition is not only dependent by the capacitors' values and the signals' frequency, but also by the resistances from the circuit.

■ AMPLIFIERS WITH FIELD-EFFECT TRANSISTORS (TEC)

■ Amplifiers with field-effect transistor (TEC) in common-source connection

Study of an amplifier with TEC-J is very similar to the one of an amplifier with TEC-MOS, therefore here is presented only an amplifier with TEC-J. A typical diagram for such an amplifier is represented in fig. 7, and its model, in which for TEC-J are used the natural parameters, is given in fig. 8.

The role of the components e_g , R_G , C_i , C_e , R_S from fig. 7 and 8 is the following: e_g - signal source, which usually is of alternative signal; T - amplifying element; R_G - equivalent internal resistance of the signal source; R_{GR} and R_D -

the TEC-J's polarization resistors; R_S - amplifier's charge (consumer); C_i, C_e - input capacitor which couples the signal mass at the amplifiers' input, respectively the output capacitor which couples the consumer's output to the charge.

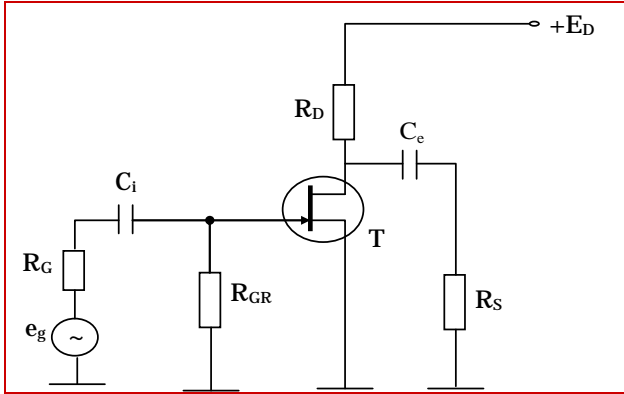


Fig. 7. Amplifier in common-source connection with TEC-J

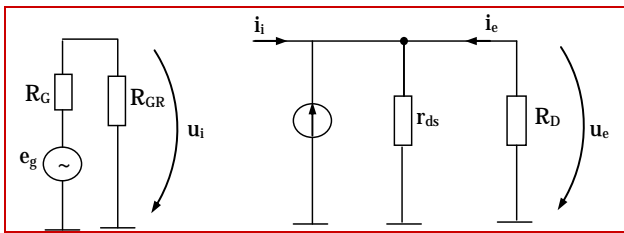


Fig. 8. Amplifier's low-signal equivalent circuit in common-source connection with TEC-J

Based on fig. 8, we have:

$$A_{us} = \frac{u_e}{u_i} = - \frac{g_m \cdot R_D}{1 + \frac{R_D}{r_{ds}}} \quad (9)$$

Because $r_{ds} \ll R_D$, the frequently used relation for the voltage amplification A_u is:

$$A_{us} = -g_m \cdot R_D \quad (10)$$

and the current amplification A_i is:

$$A_{is} = \frac{i_e}{i_i} \quad (11)$$

The current amplification is very high, but practically is less interesting because the TEC's control is made in voltage. However, a high A_i leads finally to an amplification in power A_p very high for a stage with TEC. For the input

resistance R_i and output resistance R_e , having in view the obvious neglects, are obtained:

$$R_{is} = R_{GR} \quad (12)$$

$$R_{es} = r_{ds} \quad (13)$$

Amplifiers with field-effect transistor (TEC) in common-drain connection (repeater-on-source)

The amplifier in common-drain connection (fig. 9) is useful in applications with requirements in accordance with its properties, i.e.:

- ✚ Output signal in phase with the input one;
- ✚ Very high input resistance;
- ✚ Low input capacity;
- ✚ Low output resistance;
- ✚ Output signal undeformed by high amplitude at output;
- ✚ Voltage amplification slightly subunitary.

Current amplification A_i is very high:

$$A_{id} = \frac{i_e}{i_i} \uparrow \quad (14)$$

and the voltage amplification A_u is expressed by the relation (15) and has the value closed to 1.

$$A_{ud} = \frac{g_m \cdot R_D}{1 + g_m \cdot R_D} \quad (15)$$

$$R_d = r_{ds} \parallel R_{SU} \parallel R_S \quad (16)$$

The stage's own input resistance is given practically by the value of R_{GR} which should be chosen of an as high possible value, or, in some cases, equal with the value of the signal source's equivalent resistance R_G . The stage's own output resistance is low, having the value:

$$R_{ed} = \frac{1}{g_m + \frac{1}{r_{ds}}} \quad (17)$$

and the total one R_{et} :

$$R_{etd} \cong R_S \parallel R_{SU} \quad (18)$$

The stage's total input capacity is:

$$C_{idt} = C_{gd} + (1 - A_u) \cdot C_{gs} \cong C_{gd} \quad (19)$$

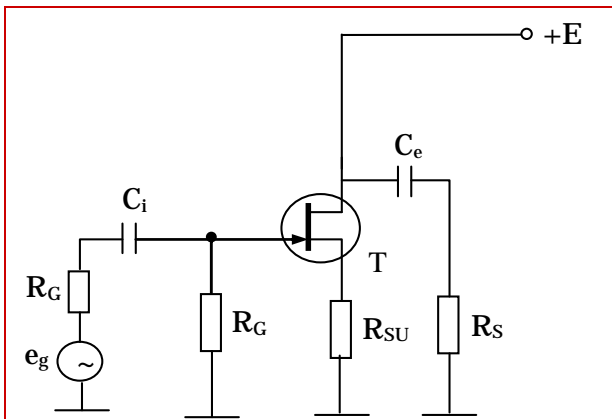


Fig. 9. Amplifier with TEC-J in common-drain connection

Amplifiers with field-effect transistor (TEC) in common-grid connection

The amplifier with TEC in common-grid connection (Fig. 10) is lesser used, and its main qualitative characteristics are the following:

- ⚡ High output impedance;
- ⚡ Low input impedance;
- ⚡ Unitary current amplification;
- ⚡ Low input → output transfer capacity;
- ⚡ The output signal is in phase with the input one.

Under mathematical aspect, the circuit's voltage amplification is:

$$A_{ug} = \frac{(1 + g_m \cdot r_{ds}) \cdot R_S}{R_S + r_{ds} + (1 + g_m \cdot r_{ds}) \cdot R_S} \approx g_m \cdot (R_S || r_{ds}) \quad (20)$$

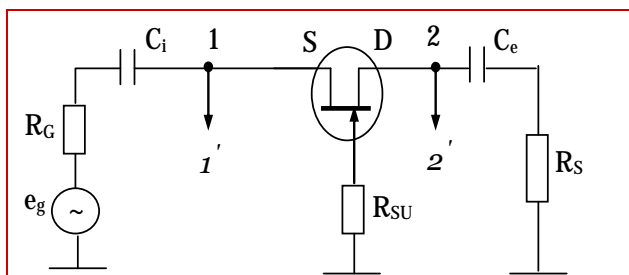


Fig. 10. Amplifier with TEC-J in common-grid connection

SIMULATION OF THE LOW-SIGNAL AMPLIFIERS' OPERATION WITH TEC USING EWB-MULTISIM 8

The amplifier with TEC-J in common-source connection is a classic one (Fig. 11). Resistors R1 and R3 achieve the automatic polarization, R3 introducing also a negative reaction in d.c. Resistor R2 represents the drain charge of the transistor T, and R_s is the amplifier's external charge.

Capacitors C1 and C2 achieve the galvanic separation of the amplifier from the signal source, respectively from the charge. The capacitor C3 decouples totally in a.c. the resistor R3 in order not to decrease the circuit's voltage amplification.

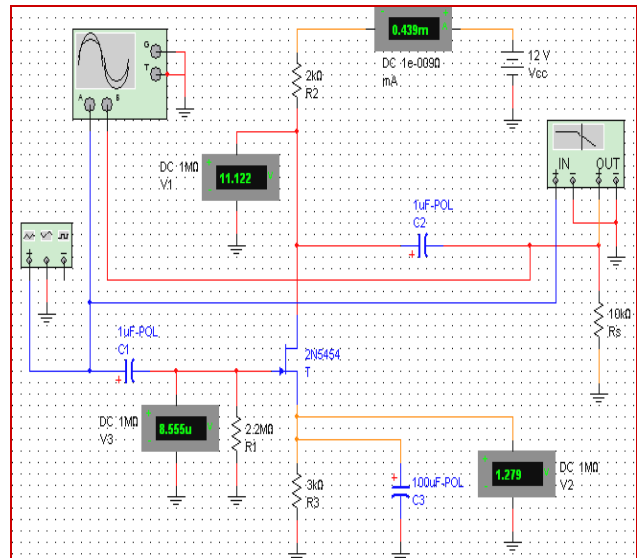


Fig. 11. The amplifier's simulation diagram with TEC-J in common-source connection

It's been achieved the simulation of this amplifier's operation for the following values of the electronic components from diagram: $S_V = 1 \text{ mV}/10 \text{ kHz}$, $V_{cc} = 12 \text{ V}$, $T = 2N5454$, $R_1 = 2,2 \text{ M}\Omega$, $R_2 = 2 \text{ k}\Omega$, $R_3 = 3 \text{ k}\Omega$, $C_1 = C_2 = 1 \mu\text{F}$, $C_3 = 100 \mu\text{F}$, $R_s = 10 \text{ k}\Omega$. Were measured: the the circuit's current consumption and the voltages in drain, the source and grid of the transistor T.

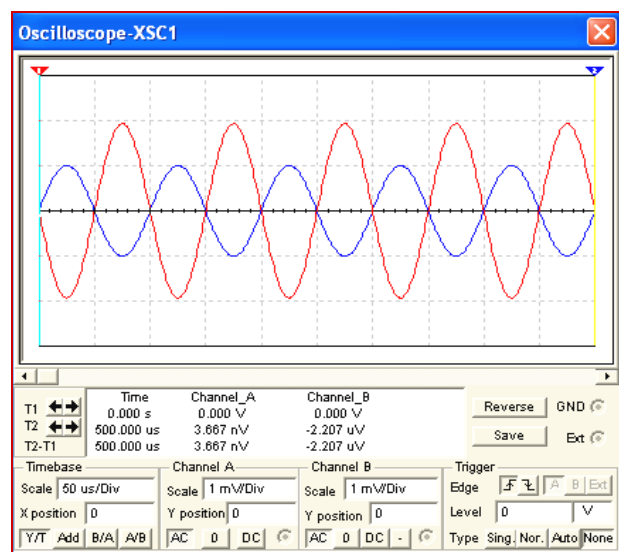


Fig. 12. Signals from the amplifier's input and output with TEC-J in common-source connection resulted further simulation

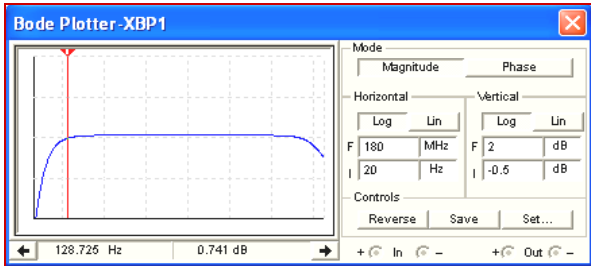


Fig. 13. Amplifier's amplitude-frequency characteristic with TEC-J in common-source connection resulted further simulation

Have been visualized on oscilloscope the signals from the amplifier's input and output with TEC-J in common-source connection (fig. 12). The amplitude-frequency characteristic of this amplifier, resulted further simulation, is presented in fig. 13.

The amplifier with TEC-MOS transistor, repeater-on-source with bootstrap reaction, (Fig. 14), represents an apart amplifier type, used especially as adaption circuit for signal sources with extremely high internal resistance. The bootstrap connection applies by the capacitor C2, which, by the the positive reaction source-grid which introduces it, increases the amplifier's input equivalent resistance (however very high in the presented case).

Resistors R1, R2 form the voltage divider from the grid of the transistor used for its polarization, and the resistor R3, of high value, has the role to ensure a high input resistance to the circuit. The resistor Rs contribute to establishing the drain current of transistor T, having in this case also the role of charge resistance.

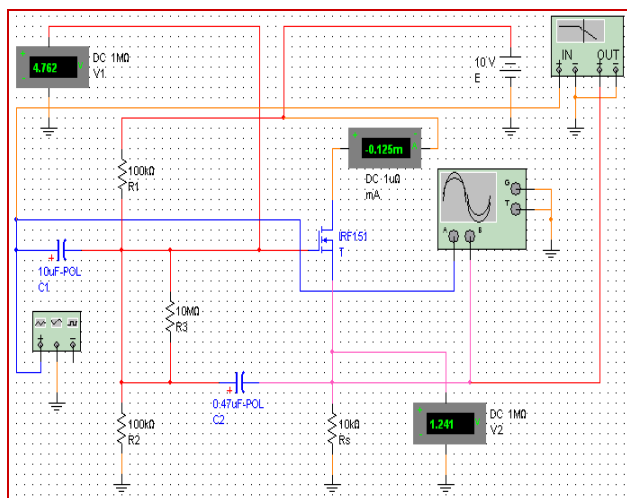


Fig. 14. Amplifier's simulation diagram with TEC-MOS in common-drain connection (repeater-on-source)

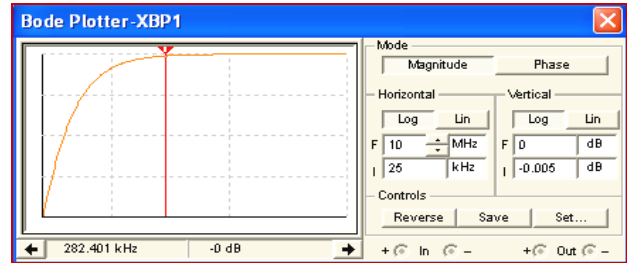


Fig. 15. The amplifier's amplitude-frequency characteristic with TEC-MOS in common-drain connection resulted further simulation

It's been achieved the simulation of this amplifier's operation for the following values of the electronic components from diagram: $S_V = 100 \text{ mV} / 10 \text{ kHz}$, $E = 10 \text{ V}$, $T = \text{IRF151}$, $R_1 = 100 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $R_3 = 10 \text{ M}\Omega$, $C_1 = 10 \text{ }\mu\text{F}$, $C_2 = 0,47 \text{ }\mu\text{F}$, $R_s = 10 \text{ k}\Omega$.

Was measured the circuit's current consumption, the grid voltage and the drain of transistor T. The amplitude-frequency characteristic of this amplifier, resulted further simulation, is presented in fig. 15.

Following the simulation, were visualized on oscilloscope the signals from the amplifier's input and output with TEC-MOS in common-drain connection (fig. 16).

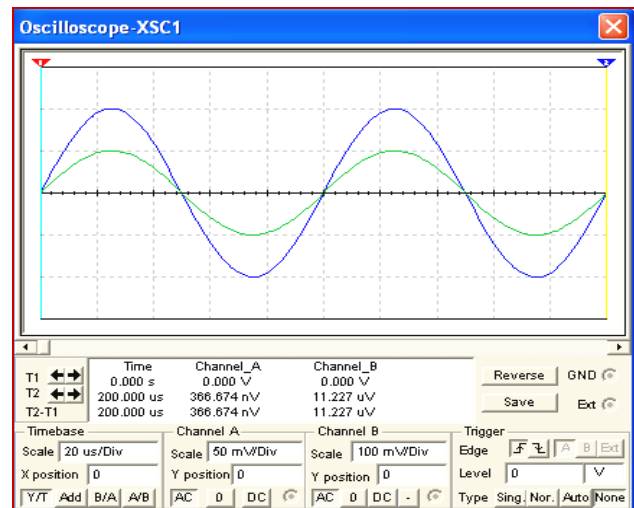


Fig. 16. Signals from the amplifier's input and output with TEC-MOS in common-drain connection resulted further simulation

The cascode amplifier with two TEC-J transistors (Fig. 17) is used especially at high frequencies. Transistor T1 works in common-source connection and transistor T2 in common-grid connection, the coupling between the two transistors being direct. Thus, are ensured the equivalent input and output specific resistances and a high voltage amplification, comparable

with the one of a classic amplifier with two amplifier stages. Resistors $R1$ and $R2$ ensure the simultaneous polarization, convenient, of transistors $T1$, $T2$.

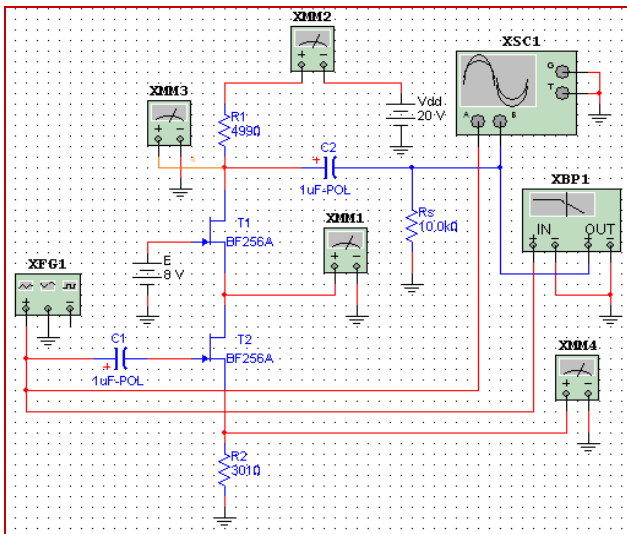


Fig. 17. Simulation diagram of the cascode amplifier with two TEC-J transistors

Capacitors $C1$, $C2$ achieve the galvanic separation between the amplifier and the $5V$ signal source (XFG1 functions generator), respectively the charge R_s .

Was achieved the simulation of this amplifier's operation for the following values of the electronic components from diagram: $5V = 1$ mV/10 kHz, $E = 8$ V, $V_{dd} = 20$ V, $T1 = BF256A$, $T2 = BF256A$, $R1 = 499 \Omega$, $R2 = 301 \Omega$, $C1 = C2 = 1 \mu F$, $R_s = 10$ k Ω .

Was measured the circuit's consumption, the voltage in the source and drain of transistor $T1$, as well as the voltage in the source and drain of transistor $T2$. The amplitude–frequency characteristic of this amplifier, resulted further simulation, is presented in fig. 18.

In fig. 19 were visualized on oscilloscope the input and output signals of the cascode amplifier with two TEC-J transistors resulted further simulation.

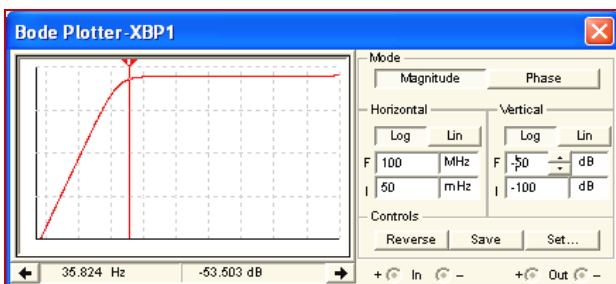


Fig. 18. The amplitude-frequency characteristic of the cascode amplifier with two TEC-J transistors

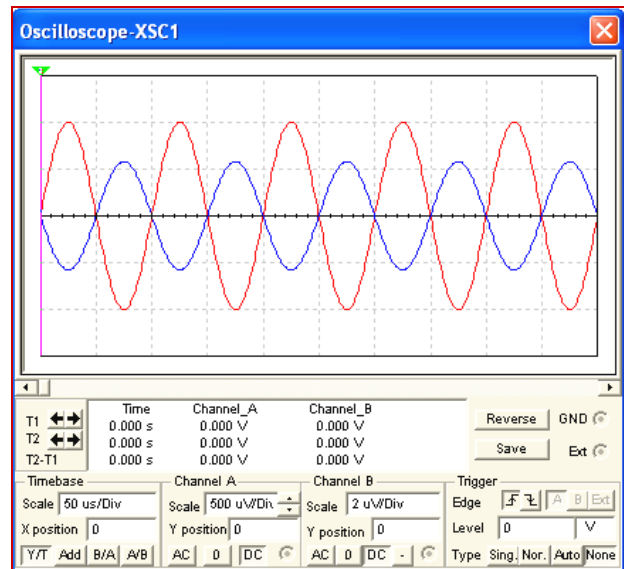


Fig. 19. Signals from the cascode amplifier's input and output with two TEC-J transistors

CONCLUSIONS

Simulation of the low-signal amplifiers' operation with field-effect transistors has a very important role, being the intermediary step absolutely necessary between designing and achievement of the experimental model. Thus, the user can observe by simulation, without being necessary the practical achievement of the electronic circuit, the real behavior and can modify certain components in order to reach the desired result.

After the electronic diagram's achievement, by software can be performed an operational analysis, as well as the behavior in different duty regimes – d.c., impulses, transitory and stationary regimes, behavior with frequencies, etc – by means of the own measurement and diagnosis systems, as well as the software's specific facilities.

The main advantage offered by the EWB–Multisim 8 simulation program consists in high flexibility as regards the structure modification of the analyzed electronic circuits and their duty regimes, fact which allows an analysis and a diagnosis within a much more reduced time interval of the electronic circuits than the case when these would be physically achieved, allowing in addition a facile and large storage of information about the circuit's operation between different implementation options.

One can notice the time savings and the possibility of further data processing, especially

the graphic dependencies for different measures, by means of the EWB–Multisim 8 program

■ **REFERENCES**

-
- [1] CĂTĂLIN DANIEL CĂLEANU, *Electronic devices and circuits, Experiments and Simulation*, „Politehnica” Publishing House, Timisoara, 2003
 - [2] THOMAS L. FLOYD, *Electronic devices*, „Teora” Publishing House, Bucharest, 2003
 - [3] E. LAKATOȘ, *Modeling of active semi-conductor devices, Course notes*, „MatrixRom” Publishing House, Bucharest, 2003
 - [4] Ș. LUNGU, O. POP, *Modeling of electronic circuits*, “Science Book House” Publishing House, Cluj-Napoca, 2006
 - [5] S. PAȘCA, N. TOMESCU, I. SZTOLJEANOV, *Analogue and digital electronics*, „Albastra” Publishing House, Cluj-Napoca, 2004

■ **AUTHORS & AFFILIATION**

¹. CORINA MARIA DINIȘ,

². CORINA DANIELA CUNTAN,

³. GABRIEL NICOLAE POPA,

⁴ ANGELA IAGĂR

^{1, 2, 3, 4}. DEPARTMENT OF ELECTRICAL ENGINEERING & INDUSTRIAL INFORMATICS,
FACULTY OF ENGINEERING HUNEDOARA,
UNIVERSITY “POLITEHNICA” TIMISOARA, ROMANIA